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# A PMOS multipled LVTSCR device for ESD protection with a higher holding voltage

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**Abstract**：A novel LVTSCR structure for 5 V on-chip protection against Electrostatic Discharge(ESD) stress at input or output pads is presented. Silvaco 2D TCAD software is used to simulate the device including electrical and thermal characteristics. The new device exchanges the diffusion region of N+ and P+ in N-WELL and introduces a PMOS-like structure to discharge ESD current before Low Voltage Triggering SCR(LVTSCR) starting to work. And the device simulation results show that it obtains a higher holding voltage(10.51 V) and a faster turn on speed($1.05\times10^{-10}$ s) compared with LVTSCR, with the triggering voltage only increasing slightly from 12.45 V to 15.35 V. Also, in order to make sure that the PMOS structure will trigger first and will not cause thermal breakdown problem, nearly the same channel length as NMOS should be chosen for PMOS structure.

**Key words**：electrostatic discharge；Low Voltage Triggering SCR；PMOS trigger；Silvaco
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In recent CMOS and BiCMOS technologies, ESD protection has a practical problem for the demand of a lower triggering voltage and a higher holding voltage within a small layout area. SCR could be used for ESD protection because of its high second breakdown current(It2) and low-capacitance[1]. But its high switching voltage has limited the use of SCR-based devices in on-chip ESD protection[2]. In order to trigger SCR at a low voltage, an NMOS structure is included in LVTSCR[3] shown in Fig.1 and Table 1. When it comes to the application of mixed-voltage interface ESD, Complementary-LVTSCR could have a good performance[4]. Also, modified lateral SCR(MLSCR) and Capacitance Coupling Triggering SCR(CCTSCR) were designed based on a lower triggering voltage strategy[5-6]. And the PMOS trigger structure is also suitable for ESD protection[7-8]. Although a lower triggering voltage is important, a higher holding voltage within an acceptable triggering voltage is more practical to avoid Latch-Up Effect. Transforming the LVTSCR at the diffusion region of N+ and P+ in N-WELL, shown in Fig.2 and Table1, can raise its holding voltage, but the triggering voltage(Vt1) will increase either. The LVTSCR and transformed LVTSCR have a same working process. First, the NMOS is brokendown and triggers the SCR structure starting to work, shown in Fig.3 and Fig.5. Then the device will reach its holding point since current rising, shown in Fig.4 and Fig.6. So another pre-triggering mechanism is needed to lower Vt1 of the transformed LVTSCR, in order to design an ESD device with better performance based on a higher holding voltage. These features about LVTSCR and PMOS are combined together with a novel multiplexed PMOS in the PMOS multipled LVTSCR(PMLVTSCR).

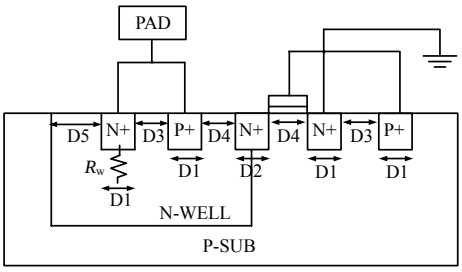


Fig.1 Structure of normal LVTSCR

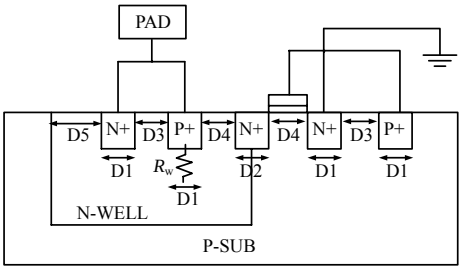


Fig.2 Structure of the transformed LVTSCR

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Table1 Layout parameters of normal LVTSCR, transformed LVTSCR and PMLVTSCR

| device name | D1/μm | D2/μm | D3/μm | D4/μm | D5/μm | D6/μm |
|---|---|---|---|---|---|---|
| normal LVTSCR | 3.6 | 2.7 | 3 | 0.65 | 1.5 | |
| transformed LVTSCR | 3.6 | 2.7 | 3 | 0.65 | 1.5 | |
| PMLVTSCR | 3.6 | 2.7 | 3 | 0.65 | 1.5 | 0.65 |

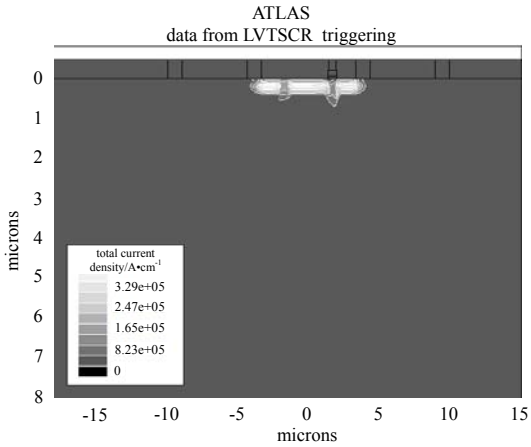


Fig.3 Current density distribution when LVTSCR was triggered

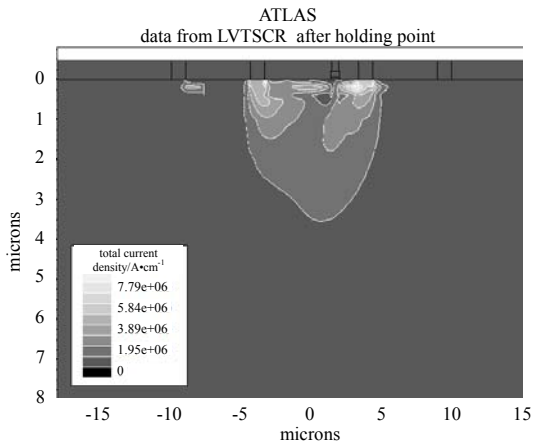


Fig.4 Current density distribution when LVTSCR reached its holding point

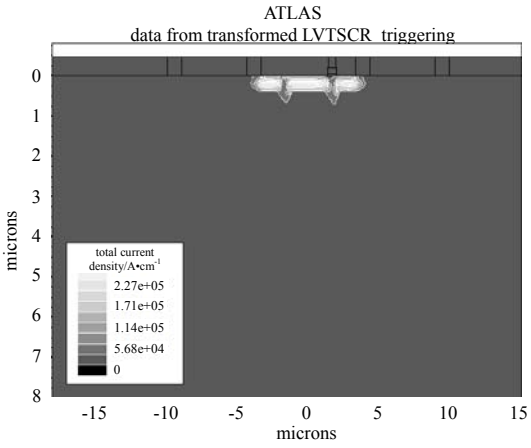


Fig.5 Current density distribution when transformed LVTSCR was triggered

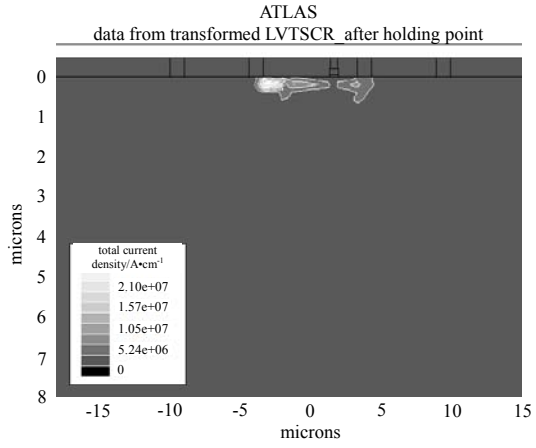


Fig.6 Current density distribution when transformed LVTSCR reached its holding point

## 1 PMLVTSCR

The PMOS transistor with a multiplexed P+ is designed into the PMLVTSCR for pre-releasing ESD pulse, shown in Fig.7, Fig.8 and Table1. In 5 V on-chip ESD protection, choosing 50 μm as the standard width of the devices, layout area only increases slightly from 1 195 $\mu m^2$ to 1 332.5 $\mu m^2$. Because the breakdown voltage of PMOS is lower than that of NMOS, PMOS will breakdown first and the PMLVTSCR's triggering point can be observed. And the PMOS will show negative resistance characteristic until it reaches its holding point. Then the PMOS will show resistance characteristic and the rising voltage will cause NMOS to breakdown. Later, the SCR structure will be triggered and start to discharge current. Compared with the transformed LVTSCR, PMOS in PMLVTSCR can help LVTSCR as an assist suppressor. Also, its current percentage will increase since SCR reaches its holding point and shows resistance characteristic. So PMLVTSCR will represent the characteristic of PMOS partially after reaching its holding point. As a result, the holding voltage will increase compared

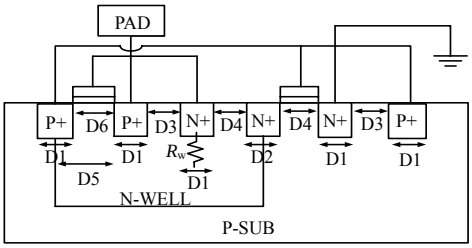


Fig.7 Structure of PMLVTSCR

with transformed LVTSCR as well. With the lattice temperature rising, the thermal breakdown of PMLVTSCR will finally occur.

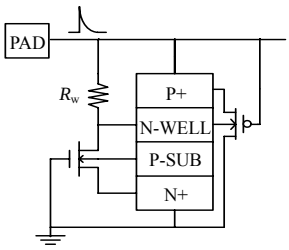

Fig.8 Equivalent circuit of PMLVTSCR

## 2 Simulation

Using the 2D device simulation tool–Atlas of Silvaco, the total current density distributions of PMLVTSCR were obtained by DC simulation. As shown in Fig.9, the PMOS will breakdown first due to the voltage rising. And the triggering point of PMLVTSCR can be observed. Since the holding point of PMOS was reached, the PMOS turned to show resistance characteristic. And the voltage on NMOS caused it to breakdown, shown in Fig.10. Then Fig.11 shows that the SCR structure will be triggered and start to discharge ESD current. Later, the SCR structure reached its holding point. As Fig.12 shown, the current percentage through PMOS will increase in the mean time. So the PMOS plays a full-time assist suppressor role though a whole ESD process.

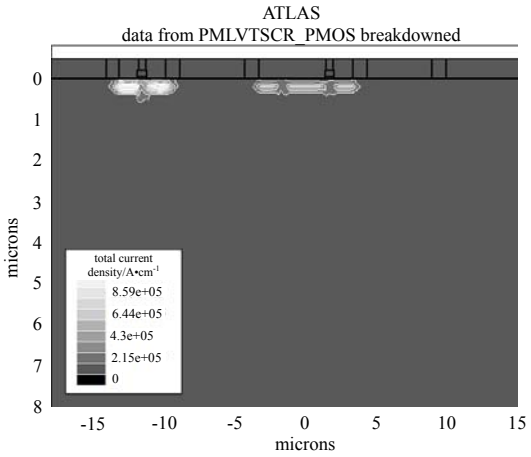

Fig.9 Current density distribution when PMOS breakdown

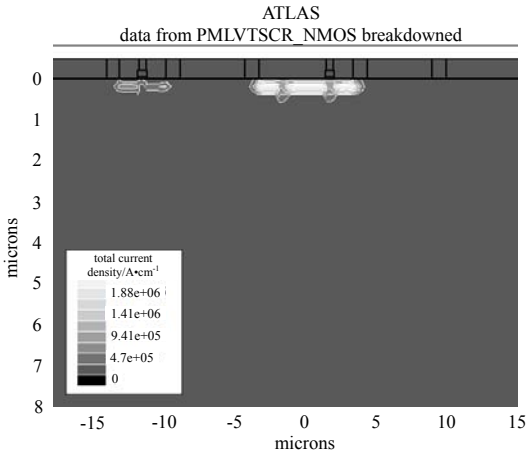

Fig.10 Current density distribution when NMOS breakdown

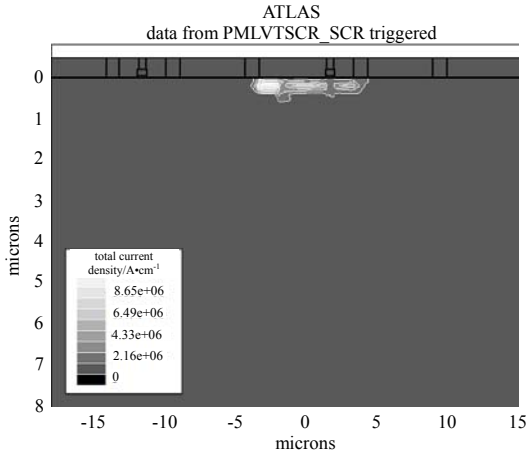

Fig.11 Current density distribution when SCR structure triggered

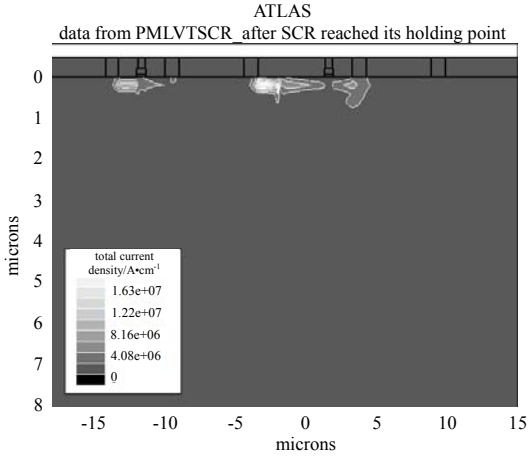

Fig.12 Current density distribution after SCR structure reached its holding point

Analyzing the I–V characteristic curves and characteristics table which are resulted from DC simulation and shown in Fig.13 and Table2, comparing them with that of the normal LVTSCR, PMOS-base LVTSCR, transformed LVTSCR and PMOS, it can be seen that the PMLVTSCR represents the highest holding voltage without increasing its triggering voltage too much. Also, the triggering current is the highest. So PMLVTSCR has a good ESD characteristic for 5 V circuit on-chip protection. In order to find out the transient response characteristics, a 30 V step voltage with a 0 s ramp time is used during transient simulation(choosing the point which has the corresponding current that equals to 80% of the highest

current as a reference point of turn on speed). As a result, Fig.14 and Table2 show that PMLVTSCR represented a faster turn on speed compared with normal LVTSCR, transformed LVTSCR and PMOS-base LVTSCR due to its PMOS structure.

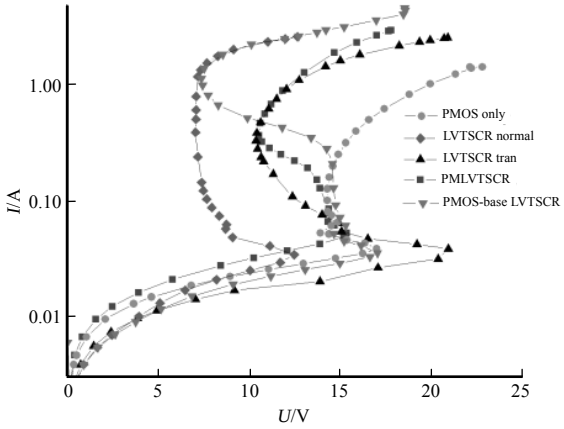


Fig.13 Simulated DC I–V curves

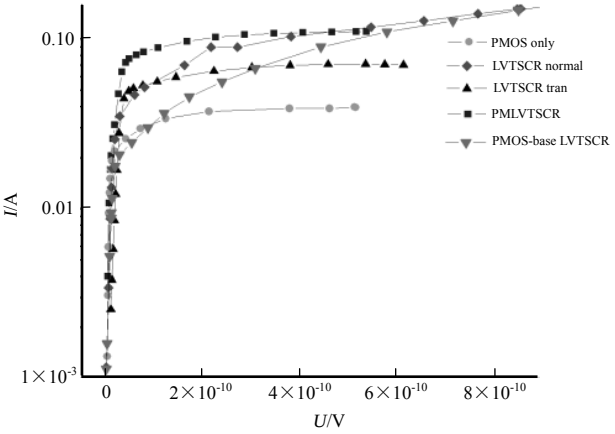


Fig.14 Transient time simulation

Table2 Characristics of PMOS, normal LVTSCR, transformed LVTSCR and PMLVTSCR

| | DC simulation | | | | transient simulation | |
|---|---|---|---|---|---|---|
| | triggering current/A | triggering voltage/V | holding current/A | holding voltage/V | highest step current/A | turn on speed/s |
| PMOS | 0.0394 7 | 16.99 | 0.053 9 | 13.900 | 0.0397 1 | $9.65\times10^{-11}$ |
| LVTSCR normal | 0.0351 1 | 12.45 | 0.399 2 | 7.029 | 0.1510 0 | $5.85\times10^{-10}$ |
| PMOS-base LVTSCR | 0.0360 9 | 17.03 | 1.161 0 | 7.368 | 0.1627 0 | $7.87\times10^{-10}$ |
| LVTSCR tran | 0.0365 4 | 21.42 | 0.338 0 | 10.370 | 0.0711 5 | $1.40\times10^{-10}$ |
| PMLVTSCR | 0.0537 0 | 15.35 | 0.423 8 | 10.510 | 0.1106 0 | $1.05\times10^{-10}$ |

Thermal rising is one of the main reasons of secondary breakdown[9]. Since the PMOS will generate heat after being triggered, the PMOS will face thermal breakdown problem. The longer the channel length of PMOS, the higher triggering voltage of PMOS will be, as shown in Fig.15. But once shorten the channel length, the PMOS's thermal breakdown problem will be the worst, as shown in Fig.16 and Fig.17. In conclusion, choosing the appropriate PMOS length which is nearly the same as that of NMOS can obtain a good ESD characteristic. The distributions of lattice temperature shown in Fig.16 proves that the highest temperature of PMLVTSCR will occur at N+ junction in N-WELL, not at the PMOS structure. This phenomenon illustrates that the appropriate PMOS, which has nearly the same channel length as NMOS, added in PMLVTSCR, will not cause thermal breakdown problem.

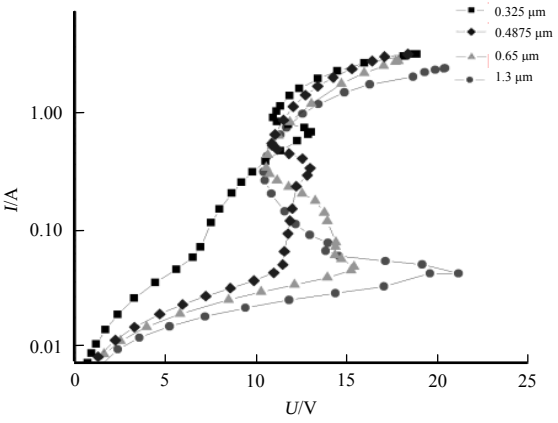


Fig.15 Simulated DC IV curves of different PMOS lengths

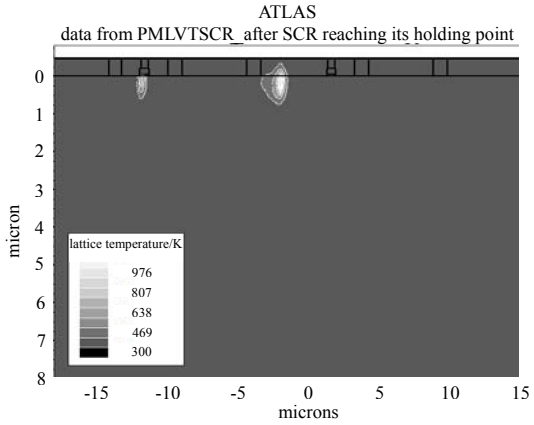


Fig.16 Lattice temperature when PMLVTSCR is thermal brokendown

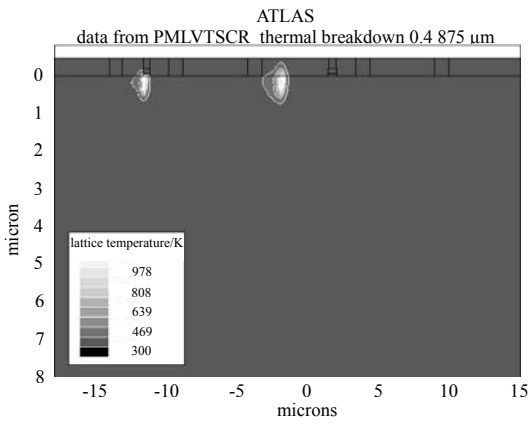


Fig.17 Lattice temperature when 0.75*D6 PMLVTSCR is thermal brokendown

## 3 Conclusion

In order to design a device that has a higher holding voltage for 5 V on-chip ESD protection circuit in a limited layout area, a PMOS structure was introduced at the region of N-WELL using a P+ of a transformed LVTSCR as a source. Atlas was used to simulate the characteristics of PMLVSCR, normal LVTSCR, transformed LVTSCR and PMOS. The I-V curves, total current density distributions and lattice temperature distributions were obtained by DC simulation. And the step response solutions were resulted from transient simulation. As a result, PMLVTSCR represented a higher holding voltage and a faster turn on speed compared with LVTSCR. The triggering voltage increased slightly from 12.45 V to 15.35 V, but it is worth for a higher holding voltage in practical using. Also, the lattice temperature distributions showed that if choosing nearly the same PMOS channel length as NMOS, the PMOS structure introduced into this novel device will not cause thermal breakdown first.

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# 一个 LVTSCR 并联 PMOS 的高维持电压 ESD 防护器件

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**摘 要：** 为了在 5 V 片上输入输出端进行静电放电(ESD)防护，提出了一种新型的 LVTSCR 结构。使用 Silvaco 2D TCAD 软件对此器件进行包含电学及热学特性的仿真。此新型器件交换了 LVTSCR 中 N-Well 的 N+、P+掺杂区并引入了一个类 PMOS 结构用来在 LVTSCR 工作前释放 ESD 电流。器件仿真结果显示，与 LVTSCR 相比，该器件获得了更高的维持电压(10.51 V)，以及更高的开启速度($1.05\times10^{-10}$ s)，同时触发电压仅仅从 12.45 V 增加到 15.35 V。并且，如果加入的 PMOS 结构选择与 NMOS 相同的沟道长度，器件不会引起热失效问题。

**关键词：** 静电放电；低压触发可控硅器件；PMOS 触发；Silvaco 软件

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# 2014（第五届）中国物联网大会隆重开幕

2014 年 4 月 1 日，2014（第五届）中国物联网大会暨国际物联网博览会在北京国际会议中心隆重开幕。本届大会由工业和信息化部、中国科学技术协会指导，中国电子学会主办、中国电子学会物联网专家委员会和物联传媒共同承办。工业和信息化部总经济师周子学先生、中国电子学会刘汝林副理事长分别为本次大会致辞。中国电子学会秘书长徐晓兰主持会议。

周总师在致辞中，详细地分析了物联网现有发展格局，以及对今后产业发展给予了建议。他指出，2013 年物联网市值已经达到了 6 000 亿元，工信部未来将从核心技术、核心领域、协调统一、信息安全等 4 个方面加强物联网建设。2013 年，中国制定的第一个物联网标准在国际上获得通过，但周总师仍然强调，当前我国物联网发展还存在高端技术不足，信息安全存在隐患，各个行业重叠、重复建设较多等一些问题。

大会第一日上午，中国电子学会副理事长、中国工程院院士，中国电子学会物联网专家委员会主任，邬贺铨先生为本届大会做了开篇专题报告，邬院士今年所做的主题报告的题目是“大智移云与物联时代”。此外，邬贺铨院士本人还担任了由研华科技董事长刘克振，微软亚洲工程院院长刘震，利尔达科技集团创始人陈贤兴，中国移动通信集团西藏有限公司副总刘巍，浙江省杭州市拱墅区委常委、北部软件园管委会书记范永晨参与讨论的“高峰对话”论坛主持。

2014(第五届)中国物联网大会现场

中国工程院院士、昆山美国杜克大学校长、武汉大学原校长刘经南院士，中国电子学会咨询与技术评测服务中心副主任王桓博士，中国电信集团公司创新业务事业部总经理，中国电子学会物联网专家委员会委员李安民先生，中国物品编码中心主任，中国电子学会物联网专家委员会委员张成海主任分别做了专题报告。

大会首日，中国电子学会秘书长徐晓兰女士来为首批物联网成果转化基地授牌，来自南京栖霞区、杭州北部软件园、利尔达物联网科技园的三位嘉宾接受了授牌。据悉，物联网成果转化基地将综合了物联网专委会多年的实践和积累，搭建起全国性的政产学研用资的交流平台，以更好地把产学研用资等各种资源整合落地，推进中国物联网产业发展。

大会主办方相关负责人对记者表示，今年的中国物联网大会还设有“可穿戴计算产业发展之路圆桌论坛及可穿戴计算产业发展高峰论坛”、“智慧生态园区建设”、“物联网应用与标准化论坛”、“物联网与传统行业的融合”、“物联网人才培养工作会议”等五大专题论坛，分别从物联网政策，技术、应用、商业模式、人才培养、投融资等角度出发，为业内人士搭建了一个交流与合作的平台。