文章编号：2095-4980(2016)03-0474-07

Evaluating logic functionality of cascaded fracturable LUTs

GUO Zhenhong[a,b], LIN Yu[a], LI Tianyi[a], JIA Rui[a,b], GAO Tongqiang[a], YANG Haigang[a]
(a.Institute of Electronics; b.University of Chinese Academy of Sciences, Chinese Academy of Sciences, Beijing 100190, China)

Abstract: Look Up Tables(LUTs) are the key components of Field-Programmable Gate Arrays(FPGAs). Many LUT architectures have been studied; nevertheless, it is difficult to quantificationally evaluate an LUT based architecture. Traditionally, dedicated efforts on specific modifications to the technology mapping tools are required for LUT architecture evaluation. A more feasible evaluation method for logic functionality is strongly required for the design of LUT architecture. In this paper, a mathematical method for logic functionality calculation is proposed and conventional and fracturable LUT architectures are analyzed. Furthermore, a cascaded fracturable LUT architecture is presented, which achieves twice logic functionality compared with the conventional LUTs and fracturable LUTs.

Key words: Field Programmable Gate Array; cascaded Look Up Tables; functionality evaluation
CLC number: TN79　　**Document code:** A　　**doi:** 10.11805/TKYDA201603.0474

LUT based FPGAs have been one of the most popular digital logic implementation media in various application domains over last decade. However, the search of new FPGA architecture remains a continuing area of research[1]. The crucial goal of these researches is the reduction of the delay, area, and power consumption, and improvement of resource utilization, routability and logic functionality of the programmable logic.

Reducing delay quantificationally is especially important as it facilitates high frequency implementation on FPGAs. In modern FPGAs, the delay is dominated by interconnects[2-3]. Modern FPGAs fracture a LUT into several sub-LUTs in order to achieve more flexible inputs and outputs, and improve logic functionality[4-6], however, later discussion will show that more inputs cause an exponential increase in LUT area. Another method is to add inter-LUT connections, where a LUT's output connects to another LUT's input via a dedicated interconnect, to avoid going through the large multiplexer before each LUT and the channels outside the logic cluster[2].

Combining the advantages of fracturable and cascaded LUTs, a new cascaded fracturable LUT architecture is proposed. The proposed LUT works as a fracturable LUT in fracturable mode. While in cascaded mode, the fractured sub-LUTs are cascaded, in order to implement different logic functionality. An SRAM controlled multiplexer is used to switch between the two modes, and a feedback path is added for cascading the sub-LUTs, which will have a negligible cost in delay and area.

Traditionally, dedicated efforts on specific modifications to the technology mapping and packing tools are required for LUT architecture evaluation[2,7-8]. In this paper, a mathematical method for logic functionality calculation is proposed. Our evaluation method shows that the proposed architecture implements twice logic functionality of conventional LUTs and fracturable LUTs.

1　Conventional LUT

In this section, a new method is employed to evaluate logic functionality of convention LUT. The definition of logic functionality and minterm used in our evaluation method refers to [9-10].

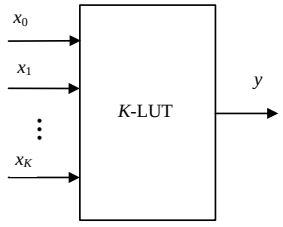

Fig.1 Conventional LUT

In Fig.1, conventional K-input LUT has K inputs and one output, which are represented by $x_i, i=1,2,\cdots,K$, and y, respectively. The LUT includes a 2^K-input multiplexer(2^K-MUX). The K inputs act as control signals of the 2^K-MUX. The inputs of the 2^K-MUX are provided by

Received date: 2014-12-01; **Revised date:** 2015-03-08
Fund project: supported by National Science and Technology Major Project of China(No. 61404140,61106033)

SRAM cells. So, the logic function of output y, $F(y)$, can be formulated as following:

$$F(y)=\alpha_0\bar{x}_1\bar{x}_2\cdots\bar{x}_K+\alpha_1\bar{x}_1\bar{x}_2\cdots\bar{x}_{K-1}x_K+\alpha_2\bar{x}_1\bar{x}_2\cdots x_{K-1}\bar{x}_K+\cdots+\alpha_{2^K-1}x_1x_2\cdots x_K \tag{1}$$

where $\alpha_i, i=0,1,\cdots,2^K-1$, are SRAM configuration bits.

$|F(y)|$ is denoted to be the number of logic functions of $F(y)$. Because there are 2^K configuration bits, the number of logic functions that conventional LUT can realize is 2^{2^K} according to Theorem 1. So the below equation is obtained:

$$|F(y)|=2^{2^K} \tag{2}$$

As the number of inputs, K, increases, the number of SRAM cells will increase exponentially, leading to a huge increase in area. Meanwhile, in practical applications, mapping logic circuits to a LUT with large number of inputs will cause lots of SRAM resources wasted.

2 Fracturable LUT

In this section, the proposed method is extended to evaluate logic functionality of fracturable LUT.

In order to increase the number of inputs and outputs, a K-LUT can be fractured into two (K–1) input sub-LUTs. The inputs of fracturable LUT are increased from K to 2K–1, and the output number is increased by 1. Each sub-LUT has 2^{K-1} SRAM cells, and total SRAM resources remain the same.

When inputs of fracturable LUT are less than 2K, some inputs are shared by the two sub-LUTs. The range of the number of shared inputs, marked as I, is from 0 to K–1. As in Fig.2, x_i, i=1,2,…,I, are shared inputs, and x_i^j, $i=I+1,\cdots,K-1$, $j=0,1$, are exclusive inputs. Each of the two sub-LUTs has its own output y^0 and y^1.

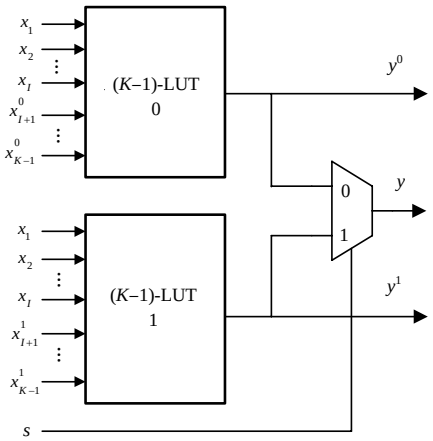

Fig.2 Fracturable LUT with shared inputs

When the fracturable LUT is used as two (K–1)–input sub-LUTs, each of them can implement $2^{2^{K-1}}$ logic functions. The logic functions of output y^j, j=0,1, are represented as following:

$$\begin{aligned}F\left(y^j\right)=&\bar{x}_1\cdots\bar{x}_I\left(\alpha_0^j\bar{x}_{I+1}^j\cdots\bar{x}_{K-1}^j+\cdots+\alpha_{2^{K-I-1}}^j x_{I+1}^j\cdots x_{K-1}^j\right)+\\&\bar{x}_1\cdots\bar{x}_{I-1}x_I\left(\alpha_{2^{K-I-1}}^j\bar{x}_{I+1}^j\cdots\bar{x}_{K-1}^j+\cdots+\alpha_{2^{K-I}-1}^j x_{I+1}^j\cdots x_{K-1}^j\right)+\cdots+\\&x_1\cdots x_{I-1}x_I\left(\alpha_{2^{K-1}-2^{K-I-1}}^j\bar{x}_{I+1}^j\cdots\bar{x}_{K-1}^j+\cdots+\alpha_{2^{K-1}-1}^j x_{I+1}^j\cdots x_{K-1}^j\right)\end{aligned} \tag{3}$$

Theorem 1: Two sub-LUTs with I shared inputs implement 2^{2^I} same logic functions.

From **Theorem 1**, the total number of same logic function of $F\left(y^0\right)$ and $F\left(y^1\right)$, represented by $\left|F\left(y^0\right)\cap F\left(y^1\right)\right|$, is 2^{2^I}. So,

$$\left|F\left(y^0\right)\right|=\left|F\left(y^1\right)\right|=2^{2^{K-1}},\left|F\left(y^0\right)\cap F\left(y^1\right)\right|=2^{2^I} \tag{4}$$

Furthermore, the two sub-LUTs can be merged by a 2-input multiplexer to generate output y. The number of logic functions that output y can realize is 2^{2^K}.

$$|F(y)|=2^{2^K} \tag{5}$$

Therefore, no matter how many inputs, the number of logic functions of output y does not change.

For output y of fracturable LUT, the number of logic functions is equal to the output of conventional LUT. However, the logic functions of the two LUT architectures are different. Conventional LUT can implement all combinational logic functions of the K inputs, however, fracturable LUT can only implement part of logic functions of all inputs.

$$\left|F(y)\right| = 2^{2^K} \tag{6}$$

3 Cascaded Fracturable LUT

Although fracturable LUT has more inputs and outputs compared to conventional LUT, the two architectures can implement same number of logic functions. In this section, a cascaded fracturable LUT architecture is proposed and its architecture is shown in Fig.3.

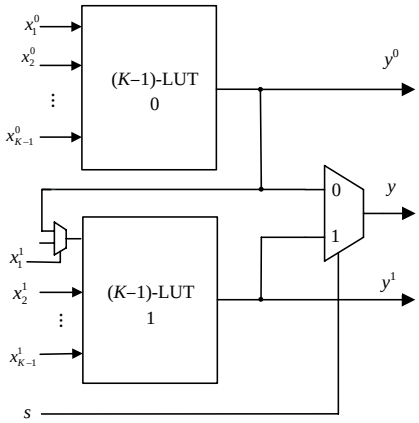

Fig.3 Proposed architecture: cascaded fracturable LUT

Compared with fracturable LUT in Fig.2, an SRAM-controlled multiplexer and a feedback path from output of LUT0 to input of LUT1 are added. By configuring the multiplexer, the proposed architecture works in two different modes, fracturable mode and cascaded mode. In fracturable mode, input x_1^1 of LUT1 is used and the feedback path is not activated, the proposed architecture acts as same as a fracturable LUT. In cascaded mode, output y^0 of LUT y^1 is used as one input to LUT1, and a LUT chain is constructed. In the following, the logic functionality of cascaded mode and fracturable mode of proposed architecture is analyzed.

3.1 Cascaded Mode

In cascaded mode, the total number of external inputs is $2K-2$ as in Fig.4, where I=0 meaning no shared inputs. LUT0 has $K-1$ external inputs, represented by x_i^0, $i=1,2,\cdots,K-1$, while LUT1 has $K-2$ external inputs, x_i^1, $i=2,3,\cdots,K-2$. And y^0 and y^1 represent the output LUT0 and LUT1 respectively, and y^0 is connected to the input of LUT1. s acts as the selection signal of the multiplexer. The logic functions of output y^1 and y can be formulated as following:

$$F\left(y^1\right) = \overline{F\left(y^0\right)}F^{'}\left(y^1\right) + F\left(y^0\right)F^{''}\left(y^1\right) \tag{7}$$

$$F\left(y\right) = \bar{s}F\left(y^0\right) + s\overline{F\left(y^0\right)}F^{'}\left(y^1\right) + sF\left(y^0\right)F^{''}\left(y^1\right) \tag{8}$$

where

$$\begin{cases} F\left(y^0\right)=\alpha_0^0\bar{x}_1^0\cdots x_{K-1}^0+\cdots+\alpha_{2^{K-1}-1}^0 x_1^0\cdots x_{K-1}^0 \\ F^{'}\left(y^1\right)=\alpha_0^1\bar{x}_2^1\cdots\bar{x}_{K-1}^1+\cdots+\alpha_{2^{K-2}-1}^1 x_2^0\cdots x_{K-1}^0 \\ F^{''}\left(y^1\right)=\alpha_{2^{K-2}}^1\bar{x}_2^1\cdots\bar{x}_{K-1}^1+\cdots+\alpha_{2^{K-1}-1}^1 x_2^0\cdots x_{K-1}^0 \end{cases}.$$

Theorem 2: The logic functions y^1 and y are $\begin{cases} F\left(y^1\right)=\overline{F\left(y^0\right)}F^{'}\left(y^1\right)+F\left(y^0\right)F^{''}\left(y^1\right) \\ F(y)=\bar{s}F\left(y^0\right)+s\overline{F\left(y^0\right)}F^{'}\left(y^1\right)+sF\left(y^0\right)F^{''}\left(y^1\right) \end{cases}$, $F\left(y^0\right), F^{'}\left(y^1\right)$ and $F^{''}\left(y^1\right)$ are the sum of products. $F\left(y^0\right)$ has N_0 configuration coefficients and N_0 complete minterms. Each of $F^{'}\left(y^1\right)$ and $F^{''}\left(y^1\right)$ has N_1 configuration coefficients. $F^{'}\left(y^1\right)$ and $F^{''}\left(y^1\right)$ have same minterms but different configuration coefficients. In each of, $F\left(y^0\right), F^{'}\left(y^1\right)$ and $F^{''}\left(y^1\right)$, only one product is 1 for any combination of its corresponding configuration coefficients. s denotes an input signal. Then the number of logic functions of y^1 and y are

$$\begin{cases} \left|F\left(y^1\right)\right| = 2^{N_1} + \left(2^{2N_1} - 2^{N_1}\right)\left(2^{N_0} - 2\right)/2 \\ \left|F\left(y\right)\right| = 2^{N_1}\times 2 + 2^{2N_1}\left(2^{N_0} - 2\right) \end{cases}.$$

In Equation 7 and Equation 8, $F\left(y^0\right)$, $F'\left(y^1\right)$ and $F''\left(y^1\right)$ have 2^{K-1}, 2^{K-2} and 2^{K-2} configuration coefficients, respectively. From **Theorem 2**, the number of logic functions of y^1 and y are

$$\left|F\left(y^1\right)\right| = 2^{2^{K-2}} + \left(2^{2^{K-1}} - 2^{2^{K-2}}\right)\left(2^{2^{K-1}} - 2\right)/2 \approx 2^{2^{K-1}} \tag{9}$$

$$\left|F(y)\right| = 2^{2^{K-2}} \times 2 + 2^{2^{K-1}}\left(2^{2^{K-1}} - 2\right) \approx 2^{2^K} \tag{10}$$

In cascaded mode, the number of inputs ranges from K to $2K-2$. When inputs are less than $2K-2$, as in Fig.4, the two sub-LUTs share I inputs, x_i, $i = 2,3,\cdots,I+1$. LUT0 has exclusive inputs represented by x_i^0, $i = 1, I+2,\cdots,K-1$, and x_i^0, $i = I+2,\cdots,K-1$, are exclusive inputs to LUT1. The logic function of output y^1 and y can be formulated as same as Equation 7 and Equation 8, but $F\left(y^1\right)$ and $F(y)$ are divided into 2^I parts according to different minterms of shared inputs. From **Theorem 2**, the following is obtained:

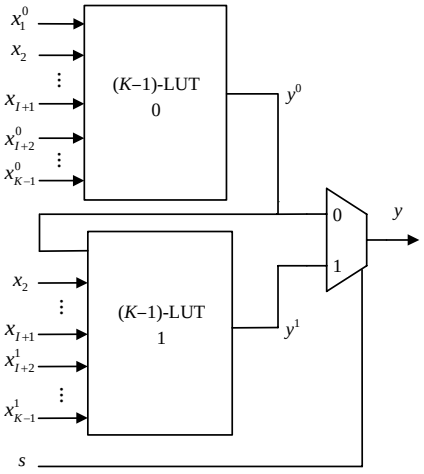

Fig.4 Cascaded mode with shared inputs

$$\left|F(y^1)\right| \approx \left(2^{2^{K-I}-1}\right)^{2^I} = 2^{2^K} - 2^I \tag{11}$$

$$\left|F(y)\right| \approx \left(2^{2^{K-I}}\right)^{2^I} = 2^{2^K} \tag{12}$$

3.2 Total logic functionality

In this subsection, the total logic functionalities of output y of the proposed architecture in both fracturable mode and cascaded mode are analyzed. $F_F(y)$ and $F_C(y)$ are used to represent the logic functions of output y in fracturable mode and cascaded mode, respectively.

From Equation 5 and Equation 12, the below equations are obtained:

$$\left|F_F(y)\right| = 2^{2^K}, \left|F_C(y)\right| \approx 2^{2^K} \tag{13}$$

However, the total number of logic functions of y is not the summation of $\left|F_F(y)\right|$ and $\left|F_C(y)\right|$, because some logic functions can be implemented both in fracturable mode and cascaded mode. $F_S(y) = F_F(y) \cap F_C(y)$ is denoted to be the same logic functions which can be implemented in the two modes, then $\left|F(y)\right|$ which represents the total number of logic functions of output y can be computed as following:

$$\left|F(y)\right| = \left|F_F(y)\right| + \left|F_C(y)\right| - \left|F_S(y)\right| \tag{14}$$

After derivation using the proposed method, the following is obtained:

$$\left|F_S(y)\right| = \left(2^{2^{K-I-1}} \times 2^{2^{K-I-2}}\right)^{2^I} = 2^{2^{K-1}} \times 2^{2^{K-2}} \tag{15}$$

$$\left|F(y)\right| \approx 2^{2^K} + 2^{2^K} - 2^{2^{K-1}} \times 2^{2^{K-2}} \approx 2^{2^K} \times 2 \tag{16}$$

4 Summary and Comparisons

As a summary of previous section, the logic functionalities of conventional LUT, fracturable LUT and the proposed cascaded fracturable LUT are summarized in Table1.

To fairly compare different LUT architectures, the same number of configurable bits, 2^K is adopted. The number of inputs to conventional LUT is K. Each sub-LUT in fracturable LUT has $K-1$ inputs, and another input is used for output selection, so totally fracturable LUT has $2K-1$ inputs. The proposed cascaded fracturable LUT also has $2K-1$ inputs. In normal mode, they works as same as inputs of fracturable LUT, while in cascaded mode, only $2K-2$ inputs are used

because one sub-LUT uses the other one's output as one of its inputs. I inputs are shared between the two sub-LUTs in fracturable LUT and the proposed architecture. Conventional LUT has 1 output, while both fracturable LUT and the proposed LUT have 3 outputs, 1 for normal mode and 2 for fracturable/cascaded mode. The number of outputs can be reduced by 1 through sharing outputs between the two modes, as in some commercial architecture.

Table1 Summary of logic functionalities of conventional LUT, fracturable LUT, and proposed cascaded fracturable LUT

		convent. LUT	fract. LUT	proposed Arch.
	#config. Bit	2^K	2^K	2^K
	#input	K	$2K-1$	$2K-1$
	#shared input	–	I	I
	#output	1	3	3
norm. mode	#output	1	1	1
	functionality	2^{2^K}	2^{2^K}	$2^{2^K}\times 2$
fracturable mode	#output	–	2	2
	functionality	–	$2^{2^{K-1}}$	$2^{2^{K-1}}$
	same function between outputs	–	2^{2^I}	2^{2^I}
cascaded mode	#output	–	–	2
	functionality	–	–	$2^{2^K-2^I}$
	same function between outputs	–	–	$2^{2^{K-1}}$

Conventional LUT implements 2^{2^K} logic functions. Fracturable LUT implements the same logic functionality in normal mode as conventional LUT does. In fractured mode, each sub-LUT implements half of the logic functionality. In the following, the logic functionalities of the proposed cascaded fracturable LUT are analyzed and compared.

4.1 Cascaded Mode

In Fig.5, the number of logic functions of cascaded mode versus the number of inputs is presented. The logic functionality of cascaded mode is normalized to 2^{2^K}, the logic functionality of conventional LUT and fracturable LUT in normal mode. A family of lines is shown and each corresponds to a LUT size in terms of configuration bits. The LUT size ranges from 2^3 to 2^{10}.

Each line in Fig.5 starts from a small value, indicates that the cascaded mode implements limited logic functionality when the two sub-LUTs share their inputs. When 2 or 3 more inputs are provided, the logic functionality increases to 1 immediately, and the cascaded mode implements the same number of logic functions as conventional LUT and fracturable LUT.

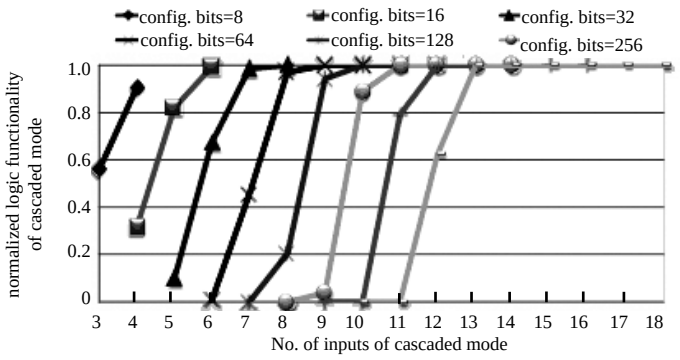

Fig.5. Logic functionality of cascaded mode

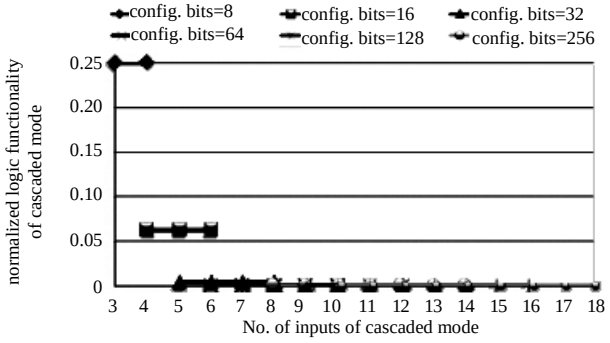

Fig.6 Same logic functionality between cascaded mode and normal mode

4.2 Same Functionality between Cascaded and Normal Node

For the proposed cascaded fracturable LUT architecture, the numbers of logic functions implemented in cascaded mode and fracturable mode are equal as in Fig.5. In Fig.6, the same logic functionality between the two modes is evaluated. The logic functionality is normalized to 2^{2^K}, the logic functionality of conventional LUT and fracturable LUT in normal mode. A family of lines of different LUT sizes is shown.

As in Fig.6, when the LUT is small, cascaded mode and fracturable mode have a large portion of same logic

functionality. The number of same functions is only related to the LUT size. When the LUT has more than 2^5 configuration bits, the same logic functionality between the two modes is very close to 0 even with limited inputs.

4.3 Total Logic Functionality

The logic functionality of cascaded mode is shown in Fig.5, and the same logic functions between cascaded mode and fracturable mode are shown in Fig.6. According to Equation 16, the total logic functionality can be computed. It can be implemented by the proposed cascaded fracturable LUT. The logic functionality is normalized to 2^{2^K}, the logic functionality of conventional LUT and fracturable LUT in normal mode.

All lines in Fig.7 representing total logic functionalities for different LUT sizes start from 1 to 1.31. Even with the two sub-LUTs sharing their inputs, the proposed cascaded fracturable LUT has the same or more logic functionality than fracturable LUT, because the cascaded mode provides more logic functionality other than fracturable mode. When 2 or 3 more inputs are provided, the total logic functionality increases immediately to 2*X* of fracturable LUT.

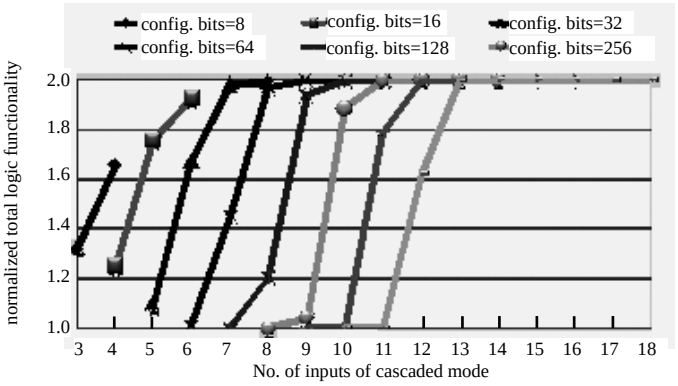

Fig.7 Total logic functionality of cascaded fracturable LUT

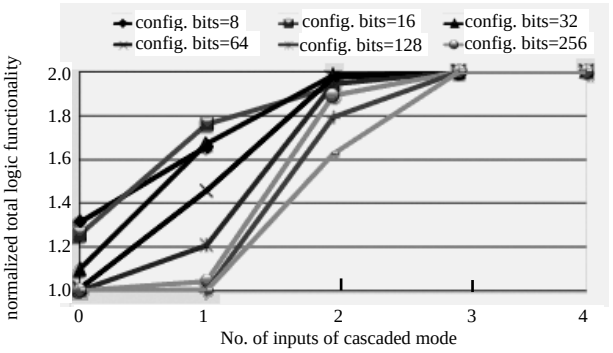

Fig.8 Total logic functionality versus No.of exclusive inputs of each sub-LUT

In order to analyze the number of extra inputs required to reach the maximum logic functionality, we drawn a family of lines representing total logic functionalities versus the number of exclusive inputs of each sub-LUT in Fig.8. When the number of exclusive inputs of each sub-LUT is 3, the total logic functionality reaches the maximum regardless of the LUT size.

5 Conclusion

In this paper, an evaluation method for logic functionality of LUT architectures is presented. Using this method, the logic functionalities of conventional LUTs and fracturable LUTs are evaluated. In order to improve the logic functionality of LUTs, a cascaded fracturable LUT architecture is proposed, and the logic functionality of this architecture is evaluated using the proposed method. Results show that the proposed architecture achieves twice logic functionality of conventional LUTs and fracturable LUTs.

References:

[1] KUON I,TESSIER R,ROSE J. FPGA architecture:Survey and challenges[J]. Foundations and Trends in Electronic Design Automation, 2008,2(2):135–253.

[2] RAY S,MISHCHENKO A,EEN N,et al. Mapping into LUT structures[C]// Proceeding of the Conference on Design, Automation and Test in Europe. Dresden:IEEE, 2012:1579–1584.

[3] MISHCHENKO A. LUT structure of delay:Cluster or cascade?[C]// International Workshop on Logic Synthesis. 2012:84–88.

[4] HUTON M D,LEWIS D,PEDERSEN B,et al. Fracturable FPGA logic elements[EB/OL]. (2006–03–01). htt:p//application-note.digchip.com/038/38–21383.pdf.

[5] LEWIS D,AHMED E,BAECKLER G,et al. The stratix II logic and routing architecture[C]// Proceeding of the ACM/ SIGDA 13th International Symposium on Field Programmable Gate Arrays. California,USA:[s.n.], 2005:14–20.

[6] ANDERSON J H,WAGN Q. Area-efficient FPGA logic elements:architecture and synthesis[C]// Proceedings of the 16th Asia and South Pacific Design Automation Conference. Yokohama:IEEE, 2011:369-375.
[7] DICKIN D,SHANNON L. Exploring FPGA technology mapping for fracturable LUT minimization[C]// 2011 International Conference on Field-Programmable Technology(FPT). New Delhi:IEEE, 2011:1-8.
[8] AHMED T,KUNDAREWICH P D,ANDERSON J H. Packing techniques for Virtex-5 FPGA[J]. ACM Transactions on Reconfigurable Technology and Systems(TRETS), 2009,2(3):18.
[9] SASAO T. Memory-Based Logic Synthesis[M]. [S.l.]:Springer, 2011.
[10] SASAO T. Switching Theory for Logic Synthesis[M]. [S.l.]:Kluwer Academic Pub., 1999.

Biography:

GUO Zhenhong(1989-), female, born in Xiangyang, Hubei Province, Master's degree. Main resarch field includes digtial IP.email: guozh827@ 126.com.

LI Tianyi(1989-), male, born in Changchun, Jilin Proving, Master's degree. Main resarch field includes mixed-signal circuit, especially design of DDR circuit.

GAO Tongqiang(1970-), male, born in Shijiazhang, Hebei Province, associate professor. Main reserach field includes CMOS radio-frequency/analog integrated circuit.

LIN Yu(1982-), male, born in Zhuhai, Guangdong Province, reserach assistant. Main research fields include architecurn of FPGA, FPGA CAD tools, high-level sythessis of FPGA and high performance computing, etc.

JIA Rui(1988-), male, born in Taiyuan, Shanxi Province, Doctor's degree. Main research field includes reconfiguable computing.

YANG Haigang(1960-), male, born in Shanghai, professor. Main research field include mixed-signal integrated circuit and very large scale integrated circuit.

* *